

## MEMORY

**CMOS 4M × 72 Bit  
FAST PAGE MODE DRAM MODULE****MB85317A-60/-70****CMOS 4M × 72 Bit Fast Page Mode DRAM Module****DESCRIPTION**

The Fujitsu MB85317A is a fully decoded, CMOS Dynamic Random Access Memory (DRAM) module consisting of eighteen MB8116400A devices. The MB85317A is optimized for those applications requiring high speed, high performance and large memory storage. The operation and electrical characteristics of the MB85317A are the same as the MB8116400A which features fast page mode operation. For ease of memory expansion, the MB85317A is offered in an 168-pad Dual In-line Memory Module package (DIMM).

**ABSOLUTE MAXIMUM RATINGS (See NOTE.)**

Parameter	Symbol	Value	Unit
Supply Voltage	V <sub>CC</sub>	-0.5 to +7.0	V
Input Voltage	V <sub>IN</sub>	-0.5 to +7.0	V
Output Voltage	V <sub>OUT</sub>	-0.5 to +7.0	V
Short Circuit Output Current	I <sub>OUT</sub>	50	mA
Power Dissipation	P <sub>D</sub>	20	W
Storage Temperature	T <sub>STG</sub>	-55 to +125	°C

**NOTE:** Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

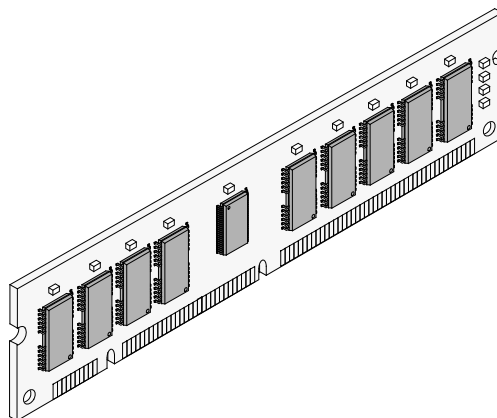
# MB85317A-60/MB85317A-70

## ■ PRODUCT LINE & FEATURES

Parameter		MB85317A-60	MB85317A-70
RAS Access Time		60 ns max.	70 ns max.
Random Cycle Time		110 ns min.	130 ns min.
Address Access Time		35 ns max.	40 ns max.
CAS Access Time		20 ns max.	22 ns max.
Fast Page Mode Cycle Time		40 ns min.	45 ns min.
Power Dissipation	Operating Mode	9020 mW max.	7920 mW max.
	Standby Mode	550 mW max.	550 mW max.

- Conformed to 8-Byte DIMM JEDEC standard
- Organization : 4,194,304 words × 72 bits (ECC)
- Module Size : 1.00" (height) × 5.25" (length) × 0.157" (thick)
- Memory : MB8116400A (4M×4, 4K ref.), 18 pcs
- TI's Input Buffers, 2pcs
- TI's Input Driver for Buffered PD, 1pc
- Decoupling Capacitors. 20pcs
- 5.0V ± 10% Supply Voltage
- 4,096 Refresh Cycles / 65.6ms
- Fast Page operation
- RAS Only Refresh / CAS-before-RAS Refresh
- Package and Ordering Information:  
168-pad DIMM, order as  
MB85317A-xxPTPBK (PTPBK = Gold Pad)

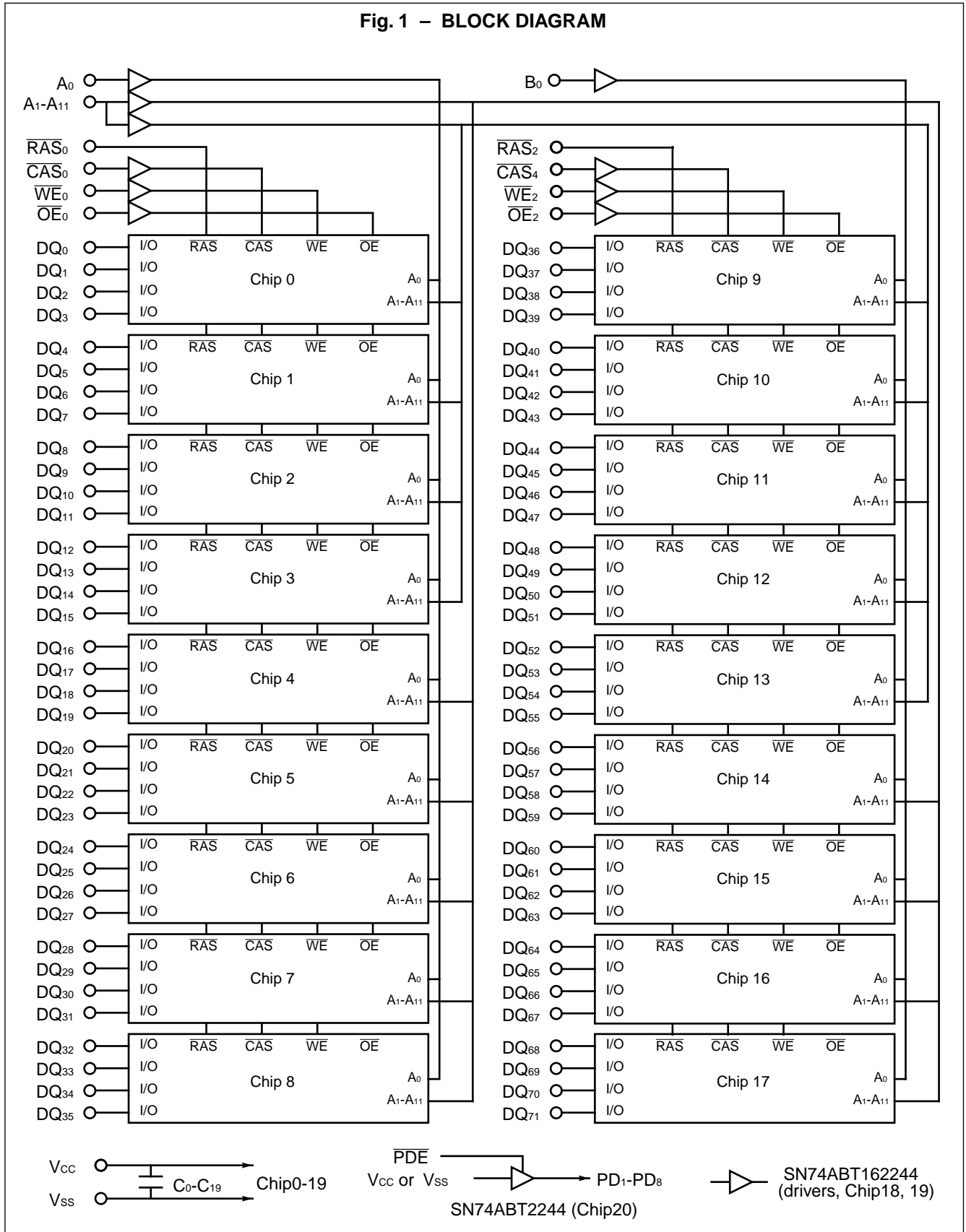
## ■ PACKAGE



MDS-168P-P04

# MB85317A-60/MB85317A-70

Fig. 1 - BLOCK DIAGRAM



# MB85317A-60/MB85317A-70

## ■ PIN ASSIGNMENTS

Pin No.	MB85317A	Pin No.	MB85317A	Pin No.	MB85317A	Pin No.	MB85317A
1	V <sub>SS</sub>	36	A <sub>6</sub>	71	DQ <sub>30</sub>	106	DQ <sub>53</sub>
2	DQ <sub>0</sub>	37	A <sub>8</sub>	72	DQ <sub>31</sub>	107	V <sub>SS</sub>
3	DQ <sub>1</sub>	38	A <sub>10</sub>	73	V <sub>CC</sub>	108	NC
4	DQ <sub>2</sub>	39	NC	74	DQ <sub>32</sub>	109	NC
5	DQ <sub>3</sub>	40	V <sub>CC</sub>	75	DQ <sub>33</sub>	110	V <sub>CC</sub>
6	V <sub>CC</sub>	41	NC	76	DQ <sub>34</sub>	111	NC
7	DQ <sub>4</sub>	42	NC	77	DQ <sub>35</sub>	112	NC
8	DQ <sub>5</sub>	43	V <sub>SS</sub>	78	V <sub>SS</sub>	113	NC
9	DQ <sub>6</sub>	44	$\overline{OE}_2$	79	PD <sub>1</sub>	114	NC
10	DQ <sub>7</sub>	45	$\overline{RAS}_2$	80	PD <sub>3</sub>	115	NC
11	DQ <sub>8</sub>	46	$\overline{CAS}_4$	81	PD <sub>5</sub>	116	V <sub>SS</sub>
12	V <sub>SS</sub>	47	NC	82	PD <sub>7</sub>	117	A <sub>1</sub>
13	DQ <sub>9</sub>	48	$\overline{WE}_2$	83	ID <sub>0</sub>	118	A <sub>3</sub>
14	DQ <sub>10</sub>	49	V <sub>CC</sub>	84	V <sub>CC</sub>	119	A <sub>5</sub>
15	DQ <sub>11</sub>	50	NC	85	V <sub>SS</sub>	120	A <sub>7</sub>
16	DQ <sub>12</sub>	51	NC	86	DQ <sub>36</sub>	121	A <sub>9</sub>
17	DQ <sub>13</sub>	52	DQ <sub>18</sub>	87	DQ <sub>37</sub>	122	A <sub>11</sub>
18	V <sub>CC</sub>	53	DQ <sub>19</sub>	88	DQ <sub>38</sub>	123	NC
19	DQ <sub>14</sub>	54	V <sub>SS</sub>	89	DQ <sub>39</sub>	124	V <sub>CC</sub>
20	DQ <sub>15</sub>	55	DQ <sub>20</sub>	90	V <sub>CC</sub>	125	NC
21	DQ <sub>16</sub>	56	DQ <sub>21</sub>	91	DQ <sub>40</sub>	126	B <sub>0</sub>
22	DQ <sub>17</sub>	57	DQ <sub>22</sub>	92	DQ <sub>41</sub>	127	V <sub>SS</sub>
23	V <sub>SS</sub>	58	DQ <sub>23</sub>	93	DQ <sub>42</sub>	128	NC
24	NC	59	V <sub>CC</sub>	94	DQ <sub>43</sub>	129	NC
25	NC	60	DQ <sub>24</sub>	95	DQ <sub>44</sub>	130	NC
26	V <sub>CC</sub>	61	NC	96	V <sub>SS</sub>	131	NC
27	$\overline{WE}_0$	62	NC	97	DQ <sub>45</sub>	132	$\overline{PDE}$
28	$\overline{CAS}_0$	63	NC	98	DQ <sub>46</sub>	133	V <sub>CC</sub>
29	NC	64	NC	99	DQ <sub>47</sub>	134	NC
30	$\overline{RAS}_0$	65	DQ <sub>25</sub>	100	DQ <sub>48</sub>	135	NC
31	$\overline{OE}_0$	66	DQ <sub>26</sub>	101	DQ <sub>49</sub>	136	DQ <sub>54</sub>
32	V <sub>SS</sub>	67	DQ <sub>27</sub>	102	V <sub>CC</sub>	137	DQ <sub>55</sub>
33	A <sub>0</sub>	68	V <sub>SS</sub>	103	DQ <sub>50</sub>	138	V <sub>SS</sub>
34	A <sub>2</sub>	69	DQ <sub>28</sub>	104	DQ <sub>51</sub>	139	DQ <sub>56</sub>
35	A <sub>4</sub>	70	DQ <sub>29</sub>	105	DQ <sub>52</sub>	140	DQ <sub>57</sub>

(Continued)

**MB85317A-60/MB85317A-70***(Continued)*

<b>Pin No.</b>	<b>MB85317A</b>	<b>Pin No.</b>	<b>MB85317A</b>	<b>Pin No.</b>	<b>MB85317A</b>	<b>Pin No.</b>	<b>MB85317A</b>
141	DQ <sub>58</sub>	148	NC	155	DQ <sub>66</sub>	162	V <sub>SS</sub>
142	DQ <sub>59</sub>	149	DQ <sub>61</sub>	156	DQ <sub>67</sub>	163	PD <sub>2</sub>
143	V <sub>CC</sub>	150	DQ <sub>62</sub>	157	V <sub>CC</sub>	164	PD <sub>4</sub>
144	DQ <sub>60</sub>	151	DQ <sub>63</sub>	158	DQ <sub>68</sub>	165	PD <sub>6</sub>
145	NC	152	V <sub>SS</sub>	159	DQ <sub>69</sub>	166	PD <sub>8</sub>
146	NC	153	DQ <sub>64</sub>	160	DQ <sub>70</sub>	167	ID <sub>1</sub>
147	NC	154	DQ <sub>65</sub>	161	DQ <sub>71</sub>	168	V <sub>CC</sub>

# MB85317A-60/MB85317A-70

## ■ PIN DESCRIPTIONS

Symbol	Function	Input/Output	Pin Count
A <sub>0</sub> to A <sub>11</sub> , B <sub>0</sub>	Address Input	Input	13
$\overline{RAS}_0$ and $\overline{RAS}_2$	Row Address Strobe	Input	2
$\overline{CAS}_0$ and $\overline{CAS}_4$	Column Address Strobe	Input	2
$\overline{WE}_0$ and $\overline{WE}_2$	Write Enable	Input	2
$\overline{OE}_0$ and $\overline{OE}_2$	Output Enable	Input	2
DQ <sub>0</sub> to DQ <sub>71</sub>	Data-input / Data-output	Input/Output	72
PD <sub>1</sub> to PD <sub>8</sub>	Presence Detect	Output	8
ID <sub>0</sub> and ID <sub>1</sub>	ID bit	Output	2
$\overline{PDE}$	Presence Detect Enable	Input	1
V <sub>CC</sub>	Power Supply	—	16
V <sub>SS</sub>	Ground	—	16
NC	No Connection	—	32

## ■ PRESENCE DETECT (PD)/ID DEFINITION

Symbol	MB85317A-60	MB85317A-70	Description of PD / ID
PD <sub>1</sub>	H	H	MODULE DENSITY, DRAM ORGANIZATION AND ADDRESSING; Module Density: 32MB, Number of Bank: 1 Bank Module Configuration: 4M ×72 Mounted DRAM Configuration: 4M ×4 DRAM Address (Row / Column): 12 / 11
PD <sub>2</sub>	H	H	
PD <sub>3</sub>	L	L	
PD <sub>4</sub>	H	H	
PD <sub>5</sub>	L	L	EDO DETECTION; Fast Page Mode : PD <sub>5</sub> = L
PD <sub>6</sub>	H	L	MODULE SPEED; 60ns : PD <sub>6</sub> = H, PD <sub>7</sub> = H 70ns : PD <sub>6</sub> = L, PD <sub>7</sub> = H
PD <sub>7</sub>	H	H	
PD <sub>8</sub>	L	L	ECC / PARITY DETECTION; ECC : PD <sub>8</sub> = L
ID <sub>0</sub>	L	L	MODULE TYPE; x72 ECC : ID <sub>0</sub> = L
ID <sub>1</sub>	L	L	REFRESH MODE; Normal Refresh : ID <sub>1</sub> = L

## ■ CAPACITANCE

(T<sub>A</sub> = 25°C, f = 1 MHz)

Parameter	Symbol	Min.	Max.	Unit
Input Capacitance, (Address)	C <sub>IN1</sub>	—	20	pF
Input Capacitance, ( $\overline{RAS}$ )	C <sub>IN2</sub>	—	80	pF
Input Capacitance, ( $\overline{CAS}$ , $\overline{WE}$ , $\overline{OE}$ )	C <sub>IN3</sub>	—	20	pF
I/O Capacitance, (DQ)	C <sub>DQ</sub>	—	20	pF

## MB85317A-60/MB85317A-70

## RECOMMENDED OPERATING CONDITION

(Referenced to  $V_{SS}$ )

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	$V_{CC}$	4.5	5.0	5.5	V
Ground	$V_{SS}$	—	0	—	V
Input High Voltage, all inputs	$V_{IH}$	2.4	—	6.0	V
Input Low Voltage, all inputs *	$V_{IL}$	-0.3	—	0.8	V
Ambient Temperature	$T_A$	0	—	70	°C

Note: \*Undershoots of up to -1.5volts with a pulse width not exceeding 10ns are acceptable.

## DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Test Condition	Symbol	Min.	Max.	Unit	
Output High Voltage *1	$I_{OH} = -5mA$	$V_{OH}$	2.4	—	V	
Output Low Voltage *1	$I_{OL} = 4.2mA$	$V_{OL}$	—	0.4	V	
Input Leakage Current	$\overline{RAS}$	$I_{I(L)}$	-50	50	$\mu A$	
	Others					-10
Output Leakage Current	$0V \leq V_{OUT} \leq 5.5V$ , $4.5V \leq V_{CC} \leq 5.5V$ , Data out disabled	$I_{O(L)}$	-10	10	$\mu A$	
Operating Current *2 (Average power supply current)	MB85317A-60	$\overline{RAS}$ & $\overline{CAS}$ cycling, $t_{RC} = \text{min.}$	$I_{CC1}$	—	1640	mA
	MB85317A-70			—	1440	
Standby Current *2 (Power supply current)	TTL Level	$\overline{RAS} = \overline{CAS} = \overline{PDE} = V_{IH}$	$I_{CC2}$	—	100	mA
	CMOS Level			$\overline{RAS} = \overline{CAS} = \overline{PDE} \geq V_{CC} - 0.2V$	—	
Refresh Current #1 *2 (Average power supply current)	MB85317A-60	$\overline{CAS} = V_{IH}$ , $\overline{RAS} = \text{cycling}$ , $t_{RC} = \text{min.}$	$I_{CC3}$	—	1640	mA
	MB85317A-70			—	1440	
Fast Page Mode Current *2	MB85317A-60	$\overline{RAS} = V_{IL}$ , $\overline{CAS} = \text{cycling}$ , $t_{PC} = \text{min.}$	$I_{CC4}$	—	1640	mA
	MB85317A-70			—	1440	
Refresh Current #2 *2 (Average power supply current)	MB85317A-60	$\overline{RAS} = \text{cycling}$ , $\overline{CAS}$ -before- $\overline{RAS}$ , $t_{RC} = \text{min.}$	$I_{CC5}$	—	1640	mA
	MB85317A-70			—	1440	

Notes: \*1 Referenced to  $V_{SS}$ .

\*2  $I_{CC}$  depends on the output load conditions and cycle rate. The specific values are obtained with the output open.

$I_{CC}$  depends on the number of address change as  $\overline{RAS} = V_{IL}$  and  $\overline{CAS} = V_{IH}$ ,  $V_{IL} > -0.3V$ .

$I_{CC1}$ ,  $I_{CC3}$  and  $I_{CC5}$  are specified at one time of address change during  $\overline{RAS} = V_{IL}$  and  $\overline{CAS} = V_{IH}$ .

$I_{CC4}$  is specified at one time of address change during one Page cycle.

# MB85317A-60/MB85317A-70

## ■ AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) Notes 1, 2, 3

No.	Parameter	Symbol	MB85317A-60		MB85317A-70		Unit	Notes
			Min.	Max.	Min.	Max.		
1	Time Between Refresh	t <sub>REF</sub>	—	65.6	—	65.6	ms	
2	Random Read/Write Cycle Time	t <sub>RC</sub>	110	—	130	—	ns	
3	Read-Modify-Write Cycle Time	t <sub>RWC</sub>	150	—	174	—	ns	
4	Access Time from $\overline{\text{RAS}}$	t <sub>RAC</sub>	—	60	—	70	ns	4,7
5	Access Time from $\overline{\text{CAS}}$	t <sub>CAC</sub>	—	20	—	22	ns	5,7
6	Column Address Access Time	t <sub>AA</sub>	—	35	—	40	ns	6,7
7	Output Hold Time	t <sub>OH</sub>	5	—	5	—	ns	
8	Output Buffer Turn On Delay Time	t <sub>ON</sub>	2	—	2	—	ns	
9	Output Buffer Turn Off Delay Time	t <sub>OFF</sub>	—	20	—	22	ns	8
10	Transition Time	t <sub>t</sub>	2	16	2	16	ns	
11	$\overline{\text{RAS}}$ Precharge Time	t <sub>RP</sub>	40	—	50	—	ns	
12	$\overline{\text{RAS}}$ Pulse Width	t <sub>RAS</sub>	60	100000	70	100000	ns	
13	$\overline{\text{RAS}}$ Hold Time	t <sub>RSH</sub>	20	—	22	—	ns	
14	$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	t <sub>CRP</sub>	5	—	5	—	ns	
15	$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	t <sub>RCD</sub>	18	40	18	48	ns	9,10
16	$\overline{\text{CAS}}$ Pulse Width	t <sub>CAS</sub>	15	—	17	—	ns	
17	$\overline{\text{CAS}}$ Hold Time	t <sub>CSH</sub>	58	—	68	—	ns	
18	$\overline{\text{CAS}}$ Precharge Time (C-B-R Refresh)	t <sub>CPN</sub>	10	—	10	—	nss	17
19	Row Address Setup Time	t <sub>ASR</sub>	5	—	5	—	ns	
20	Row Address Hold Time	t <sub>RAH</sub>	8	—	8	—	ns	
21	Column Address Setup Time	t <sub>ASC</sub>	0	—	0	—	ns	
22	Column Address Hold Time	t <sub>CAH</sub>	15	—	15	—	ns	
23	Column Address Hold Time from $\overline{\text{RAS}}$	t <sub>AR</sub>	33	—	33	—	ns	
24	$\overline{\text{RAS}}$ to Column Address Delay Time	t <sub>RAD</sub>	13	25	13	30	ns	11
25	Column Address to $\overline{\text{RAS}}$ Lead Time	t <sub>RAL</sub>	35	—	40	—	ns	
26	Column Address to $\overline{\text{CAS}}$ Lead Time	t <sub>CAL</sub>	30	—	35	—	ns	
27	Read Command Setup Time	t <sub>RCS</sub>	0	—	0	—	ns	
28	Read Command Hold Time Referenced to $\overline{\text{RAS}}$	t <sub>RRH</sub>	-2	—	-2	—	ns	12
29	Read Command Hold Time Referenced to $\overline{\text{CAS}}$	t <sub>RCH</sub>	0	—	0	—	ns	12



## MB85317A-60/MB85317A-70

## ■ AC CHARACTERISTICS (Continued)

(At recommended operating conditions unless otherwise noted.) Notes 1, 2, 3

No.	Parameter	Symbol	MB85317A-60		MB85317A-70		Unit	Notes
			Min.	Max.	Min.	Max.		
30	Write Command Setup Time	t <sub>WCS</sub>	0	—	0	—	ns	13,18
31	Write Command Hold Time	t <sub>WCH</sub>	15	—	15	—	ns	
32	Write Command Hold Time from RAS	t <sub>WCR</sub>	33	—	33	—	ns	
33	$\overline{\text{WE}}$ Pulse Width	t <sub>WP</sub>	15	—	15	—	ns	
34	Write Command to $\overline{\text{RAS}}$ Lead Time	t <sub>RWL</sub>	20	—	22	—	ns	
35	Write Command to $\overline{\text{CAS}}$ Lead Time	t <sub>CWL</sub>	15	—	17	—	ns	
36	DIN Setup Time	t <sub>DS</sub>	-2	—	-2	—	ns	
37	DIN Hold Time	t <sub>DH</sub>	20	—	20	—	ns	
38	Data Hold Time from $\overline{\text{RAS}}$	t <sub>DHR</sub>	35	—	35	—	ns	
39	$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time	t <sub>RWD</sub>	78	—	90	—	ns	18
40	$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time	t <sub>CWD</sub>	35	—	39	—	ns	18
41	Column Address to $\overline{\text{WE}}$ Delay Time	t <sub>AWD</sub>	50	—	57	—	ns	18
42	$\overline{\text{RAS}}$ Precharge Time to $\overline{\text{CAS}}$ Active Time (Refresh Cycles)	t <sub>RPC</sub>	3	—	3	—	ns	
43	$\overline{\text{CAS}}$ Setup Time (C-B-R Refresh)	t <sub>CSR</sub>	5	—	5	—	ns	
44	$\overline{\text{CAS}}$ Hold Time (C-B-R Refresh)	t <sub>CHR</sub>	8	—	10	—	ns	
45	$\overline{\text{WE}}$ Setup Time from $\overline{\text{RAS}}$	t <sub>WSR</sub>	5	—	5	—	ns	
46	$\overline{\text{WE}}$ Hold Time from $\overline{\text{RAS}}$	t <sub>WHR</sub>	8	—	8	—	ns	
47	Access Time from $\overline{\text{OE}}$	t <sub>OEA</sub>	—	20	—	22	ns	7
48	Output Buffer Turn Off Delay from $\overline{\text{OE}}$	t <sub>OEZ</sub>	—	20	—	22	ns	8
49	$\overline{\text{OE}}$ to $\overline{\text{RAS}}$ Lead Time for Valid Data	t <sub>OEL</sub>	10	—	12	—	ns	
50	$\overline{\text{WE}}$ Hold Time Referenced to $\overline{\text{WE}}$	t <sub>OEH</sub>	5	—	5	—	ns	14
51	$\overline{\text{OE}}$ to Data in Delay Time	t <sub>OED</sub>	20	—	22	—	ns	
52	$\overline{\text{CAS}}$ to Data in Delay Time	t <sub>CDD</sub>	20	—	22	—	ns	
53	DIN to $\overline{\text{CAS}}$ Delay Time	t <sub>DZC</sub>	-2	—	-2	—	ns	15
54	DIN to $\overline{\text{OE}}$ Delay Time	t <sub>DZO</sub>	-2	—	-2	—	ns	15
55	Fast Page Mode $\overline{\text{RAS}}$ Pulse Width	t <sub>RASP</sub>	—	100000	—	100000	ns	
56	Fast Page Mode Read/Write Cycle Time	t <sub>PC</sub>	40	—	45	—	ns	

# MB85317A-60/MB85317A-70

## ■ AC CHARACTERISTICS (Continued)

(At recommended operating conditions unless otherwise noted.) Notes 1, 2, 3

No.	Parameter	Symbol	MB85317A-60		MB85317A-70		Unit	Notes
			Min.	Max.	Min.	Max.		
57	Fast Page Mode Read-Modify-Write Cycle Time	$t_{PRWC}$	80	—	89	—	ns	
58	Access Time from $\overline{CAS}$ Precharge	$t_{CPA}$	—	40	—	45	ns	7, 16
59	Fast Page Mode $\overline{CAS}$ Precharge Time	$t_{CP}$	10	—	10	—	ns	
60	Fast Page Mode $\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	$t_{RHCP}$	40	—	45	—	ns	
61	Fast Page Mode $\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time	$t_{CPWD}$	55	—	62	—	ns	18

## MB85317A-60/MB85317A-70

- Notes: 1. An initial pause ( $\overline{\text{RAS}}=\overline{\text{CAS}}=V_{IH}$ ) of 200 $\mu\text{s}$  is required after power-up followed by any eight  $\overline{\text{RAS}}$ -only cycles before proper device operation is achieved. If an internal refresh counter is used, a minimum of eight  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  initialization cycles are required instead of eight  $\overline{\text{RAS}}$  cycles.
2. AC characteristics assume  $t_t = 5\text{ns}$ .
  3.  $V_{IH}$  (min.) and  $V_{IL}$  (max.) are reference levels for measuring the timing of input signals. Transition times are measured between  $V_{IH}$  (min.) and  $V_{IL}$  (max.).
  4. Assumes that  $t_{RCD} \leq t_{RCD}(\text{max.})$ ,  $t_{RAD} \leq t_{RAD}(\text{max.})$ . If  $t_{RCD}$  is greater than the maximum recommended value shown in this table,  $t_{RAC}$  will be increased by the amount that  $t_{RCD}$  exceeds the value shown.
  5. If  $t_{RCD} \geq t_{RCD}(\text{max.})$ ,  $t_{RAD} \geq t_{RAD}(\text{max.})$ , and  $t_{ASC} \geq t_{AA} - t_{CAC} - t_t$ , access time is  $t_{CAC}$ .
  6. If  $t_{RAD} \geq t_{RAD}(\text{max.})$  and  $t_{ASC} \leq t_{AA} - t_{CAC} - t_t$ , access time is  $t_{AA}$ .
  7. Measured with a load equivalent to two TTL loads and 100 pF.
  8.  $t_{OFF}$  is specified that output buffer change to high impedance state.
  9. Operation within the  $t_{RCD}(\text{max.})$  limit ensures that  $t_{RAC}(\text{max.})$  can be met.  $t_{RCD}(\text{max.})$  is specified as a reference point only; if  $t_{RCD}$  is greater than the specified  $t_{RCD}(\text{max.})$  limit, access time is controlled exclusively by  $t_{CAC}$  or  $t_{AA}$ .
  10.  $t_{RCD}(\text{min.}) = t_{RAH}(\text{min.}) + 2t_t + t_{ASC}(\text{min.})$ .
  11. Operation within the  $t_{RAD}(\text{max.})$  limit ensures that  $t_{RAC}(\text{max.})$  can be met.  $t_{RAD}(\text{max.})$  is specified as a reference point only; if  $t_{RAD}$  is greater than the specified  $t_{RAD}(\text{max.})$  limit, access time is controlled exclusively by  $t_{CAC}$  or  $t_{AA}$ .
  12. Either  $t_{RRH}$  or  $t_{RCH}$  must be satisfied for a read cycle.
  13.  $t_{WCS}$  is specified as a reference point only. If  $t_{WCS} \geq t_{WCS}(\text{min.})$  the data output pin will remain High-Z state through entire cycle.
  14. Assumes that  $t_{WCS} < t_{WCS}(\text{min.})$ .
  15. Either  $t_{DZC}$  or  $t_{DZO}$  must be satisfied.
  16.  $t_{CPA}$  is access time from the selection of a new column address (caused by changing  $\overline{\text{CAS}}$  from "L" to "H"). Therefore, if  $t_{CP}$  become long,  $t_{CPA}$  also become longer than  $t_{CPA}(\text{max.})$ .
  17. Assumes that  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh.
  18.  $t_{WCS}$ ,  $t_{CWD}$ ,  $t_{RWD}$ ,  $t_{AWD}$ , and  $t_{CPWD}$  are not restrictive operating parameters. They are included in the data sheet as an electrical characteristic only. If  $t_{WCS} \geq t_{WCS}(\text{min.})$ , the cycle is an early write cycle and Dout pin will maintain high impedance state throughout the entire cycle. If  $t_{CWD} \geq t_{CWD}(\text{min.})$ ,  $t_{RWD} \geq t_{RWD}(\text{min.})$ ,  $t_{AWD} \geq t_{AWD}(\text{min.})$ , and  $t_{CPWD} \geq t_{CPWD}(\text{min.})$ , the cycle is a read-modify-write cycle and data from the selected cell will appear at the Dout pin. If neither of the above conditions is satisfied, the cycle is a delayed write cycle and invalid data will appear the Dout pin, and write operation can be executed by satisfying  $t_{RWL}$ ,  $t_{CWL}$ ,  $t_{RAL}$  and  $t_{CAL}$  specifications.

\*Source: See MB8116400A Data Sheet for details on the electricals.



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